USN | | | | | | | | | | |

10EC751

Seventh Semester B.E. Degree Examination, May 2017
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With a neat block diagram and timing diagram explain digital signal processing system. **(08 Marks)**

b. Write a MATLAB program to obtain magnitude and phase response of the FIR filter
$y(n) = x(n) - x(n-1)$ **(06 Marks)**

c. Explain the decimation and interpolation process with an example. **(06 Marks)**

2 a. What is the role of a shifter in DSP? Explain the implementation of 4 bit shift right barrel shifter with a diagram. **(06 Marks)**

b. Explain circular and bit reversed addressing modes. **(08 Marks)**

c. Identify the addressing modes of the operands and explain their operation:
(i) ADD reg (ii) ADD mem (iii) ADD –* addreg
(iv) ADD offset reg –, * addreg (v) ADD * addreg + (vi) ADD * addreg, offset reg +
(06 Marks)

3 a. With a neat block diagram explain the multiplier and accumulate (MAC) unit of TMS320C54X processor. **(06 Marks)**

b. Draw the memory map for the TMS320C54X processor and explain processor bits for configuring the onchip memories. **(08 Marks)**

c. Assuming the current contents of AR3 to be 200h, what will be its contents after each of the following TMS320C54XX addressing modes? Assume that the contents of AR0 are 20h
(i) * AR3 + 0 (ii) * +AR3 (– 40h) (iii) * AR3 + 0B
(iv) * AR3 – 0B (v) * AR3 + (vi) * AR3 **(06 Marks)**

4 a. Explain the operation of the following instructions of TMS320C54X processor with an example:
(i) MAC (ii) RPT (iii) MPY **(06 Marks)**

b. Show the pipeline operation of the following sequence of instructions if the initial value of AR3 is 80 and the values stored in memory location 80, 81, 82, are 1, 2 and 3.

```
LD   * AR3 +, A
ADD  #1000h , A
STL  A, * AR3 +
```

(07 Marks)

c. Write a program to find the sum of a series of signed numbers stored at successive locations in the data memory and place the result in the accumulator A, i.e.,

$$A = \sum_{i=410h}^{410h} dmad(i)$$

(07 Marks)

PART – B

5 a. Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16 bit fixed point number N = 4000h in Q15, Q10, Q7 notations? **(10 Marks)**

b. Explain how the FIR filter algorithms can be implemented using TMS320C54XX processor. **(10 Marks)**

6 a. Explain a general DITFFT butterfly in place computation structure. **(04 Marks)**

b. Derive the optimum scaling factor for the DITFFT butterfly. **(08 Marks)**

c. Write an assembly language program for implementing following on TMS320C54XX processor :

(i) Bit reversed address generation

(ii) Spectrum of the transformed data **(08 Marks)**

7 a. With a neat flowchart explain handling of interrupt by TMS320C54XX processor. **(08 Marks)**

b. Design a data memory system with address range 000800h – 000FFFh for a TMS320C54XX processor. Use 2k × 8 SRAM memory chips. **(06 Marks)**

c. Explain register sub addressing technique for configuring DMA operation. **(06 Marks)**

8 a. With a neat block diagram explain the CODEC interface circuit. **(10 Marks)**

b. With the help of block diagram explain the clipping autocorrelation pitch detector. **(10 Marks)**

* * * * *